CLAIMS

What is claimed is:

1.   A method used in the generation of Reed Solomon parity bytes utilizing multiple operations some of which are comprised of the following steps:

       providing an operand representing N feedback terms where N is greater than one;

       computation of N by M Galios Field polynomial multiplications where M is greater than one; and;

       computation of (N-1) by M Galios Field additions producing M result bytes.

2.   A method recited in Claim 1, wherein said values of N and M are both the value of four resulting in computation of sixteen Galios Field polynomial multiplications.

3.   A method recited in Claim 1, wherein said computation of N by M Galios Field Polynomial multiplications occurs concurrently.

4.   A method recited in Claim 1, wherein said computation of N by M Galios Field Polynomial multiplications occurs sequentially in a pipeline.

5.   A method recited in Claim 1, wherein result bytes are used to modify Reed Solomon parity bytes in a separate operation.

6.   A method recited in Claim 1, wherein result bytes are used to modify Reed Solomon parity bytes in a same operation.

7.   A method recited in Claim 1, wherein each said Galios Field polynomial multiplication utilizes a coefficient delivered from a memory device.

8.   A method recited in Claim 7, where in said memory device include one or more elements of a group consisting of read only memory (ROM), random access memory (RAM) and a register file.

9.   A method used in the generation of Reed Solomon parity bytes utilizing multiple operations some of which are comprised of the following steps:

    providing an operand representing N feedback terms where N is greater than one;

    providing an operand representing M incoming Reed Solomon parity bytes where M is greater than one;

    computation of N by M Galios Field polynomial multiplications; and;

    computation of N by M Galios Field additions producing M modified Reed Solomon parity bytes.

10.   A method recited in Claim 9, wherein said values of N and M are both the value of four resulting in computation of sixteen Galios Field polynomial multiplications.

11.   A method recited in Claim 9, wherein said generation of Reed Solomon parity bytes requires several iterations each time using previous modified Reed Solomon parity bytes as incoming Reed Solomon parity bytes.

12.   A method used in the generation of Reed Solomon syndrome bytes utilizing multiple operations some of which are comprised of the following steps:

    providing an operand representing N data terms where N is one or greater;

    providing an operand representing M incoming Reed Solomon syndrome bytes where M is greater than one;

    computation of N by M Galios Field polynomial multiplications; and;

    computation of N by M Galios Field additions producing M modified Reed Solomon syndrome bytes.

13.   A method recited in Claim 12, wherein said values of N and M are both the value of four resulting in computation of sixteen Galios Field polynomial multiplications.

14.   A method recited in Claim 12, wherein said computation of N by M Galios Field Polynomial multiplications occurs concurrently.

15.   A method recited in Claim 12, wherein said computation of N by M Galios Field Polynomial multiplications occurs sequentially in a pipeline.

16.   A method recited in Claim 12, wherein said generation of Reed Solomon syndrome bytes requires several iterations each time using previous modified Reed Solomon syndrome bytes as incoming Reed Solomon syndrome bytes.

17.   A method recited in Claim 12, wherein each said Galios Field polynomial multiplication utilizes a coefficient delivered from a memory device.

18.   A method recited in Claim 17, wherein said memory device include one or more elements of a group consisting of read only memory (ROM), random access memory (RAM) and a register file.

19.   A method recited in Claim 17, wherein each said coefficient is derived using distributive and associative properties of Galios Field operations.

20.   A method used to simplify coefficients used in a parallelized Reed Solomon decoder comprising:

      expanding formulas for syndrome byte operations;

      applying distributive and associative properties of Galios Field operations;

      grouping multiple constants together using the same multiple type Galios Field operation; and;

forming a single aggregate constant in place of multiple constants and multiple operations.

21.   An apparatus used for the generation of Reed Solomon parity bytes implemented in digital logic performing an operation which is comprised of the following:

means for providing an operand representing N feedback terms where N is greater than one;

means for computation of N by M Galios Field polynomial multiplications where M is greater than one; and;

means for computation of (N-1) by M Galios Field additions producing M result bytes.

22.   An apparatus used in the generation of Reed Solomon parity bytes implemented in digital logic performing an operation which is comprised of the following:

means for providing an operand representing N feedback terms where N is greater than one;

means for providing an operand representing M incoming Reed Solomon parity bytes where M is greater than one;

means for computation of N by M Galios Field polynomial multiplications; and;

means for computation of N by M Galios Field additions producing M modified Reed Solomon parity bytes.

23.   An apparatus used in the generation of Reed Solomon syndrome bytes implemented in digital logic performing an operation which is comprised of the following:

means for providing an operand representing N data terms where N is one or greater;

means for providing an operand representing M incoming Reed Solomon syndrome bytes where M is greater than one;

means for computation of N by M Galios Field polynomial multiplications; and;

means for computation of N by M Galios Field additions producing M modified Reed Solomon syndrome bytes.